SCOPE — Symbolic Computation–Memory Optimization for Pipeline Efficiency in ultra-scale DNN training

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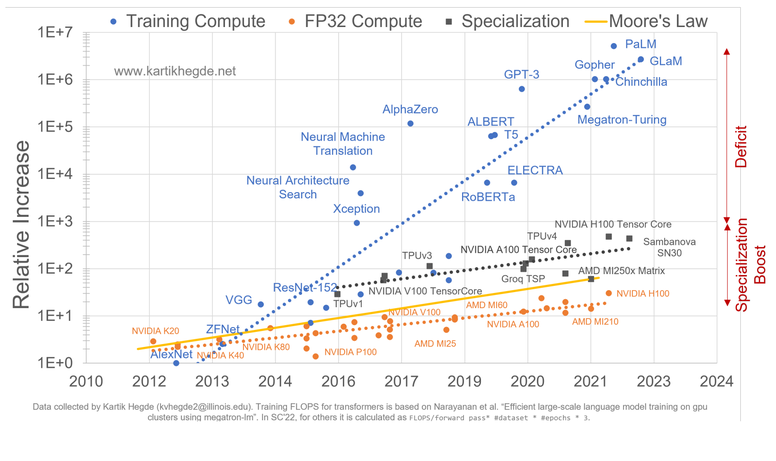
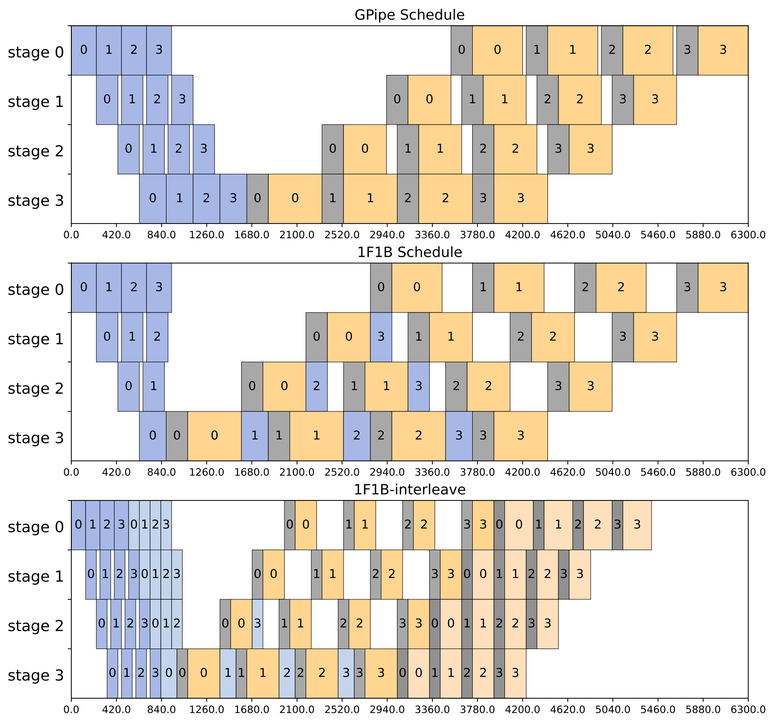
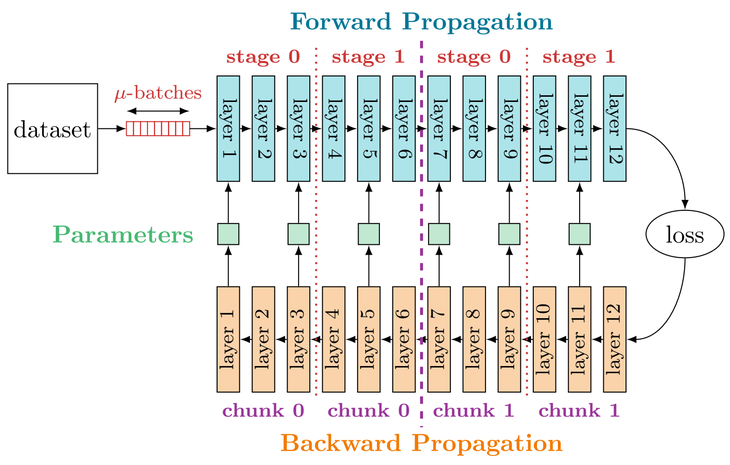
Background



- DNN models increase exponentially, making single-device training impossible.
- **Pipeline parallelism** and **activation recomputation** are widely adopted optimization techniques to scale DNN training on large accelerator clusters.

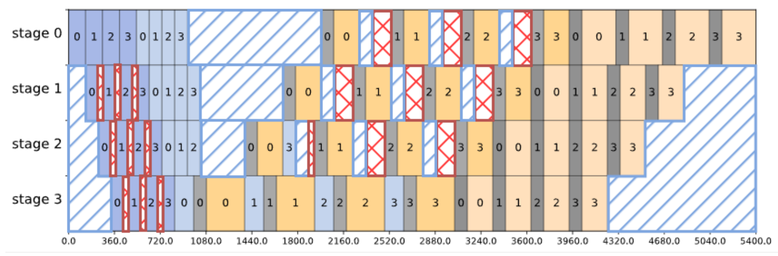


Execution scheduling has progressed from *GPipe* [1]'s fill drain to *PipeDream* [2]'s memory saving 1F1B and *Megatron* [3]'s finer-grained **1F1B interleaved schedule**, squeezing bubbles further with more complexity in the computation and memory behavior of each stage.



Pipeline schedules power large DNN training: pipeline interleave training today's multi-billion-parameter models hinges on pipeline parallelism, which slices the network into stages/chunks and streams μ-sized micro-batches, thus forward and backward passes overlap, trimming per-device memory and latency.

Motivation



The pipeline leaks three kinds of idle "bubbles":

- **recomputation** (gray blocks)
- **computation imbalance** (red blocks)
- **warm-up/cool-down preparation** (blue blocks)

State-of-the-art planners tackle bubbles piecemeal:

- *PipeDream* for imbalance computation
- *BPipe* [4] for imbalance activation memory
- *Merak* [5] for recompute
- *AdaPipe [6]* for recompute and imbalance computation
- *Zero-Bubble* [7] for preparation

SOTAs modeling only a subset of the intertwined axes of computation, memory, stages, and chunks. The prior techniques are **orthogonal**, and naively stacking them often leads to negative interference.

A holistic planner must reason about all three bubble categories under a **unify cost model**

System Design

Abstraction:

$$S^* = \begin{bmatrix} S^0 \\ S^1 \\ \vdots \\ S^{P-1} \end{bmatrix} = \begin{bmatrix} [H, l^r_0, l^r_1, ...] \dots [l^r_{j_0}, l^r_{j_0+1}, ...] \\ [l^r_{i_1}, l^r_{i_1+1}, ...] \dots [l^r_{j_1}, l^r_{j_1+1}, ...] \\ \vdots \\ [l^r_{i_{P-1}}, ...] \quad \dots \quad [..., l^r_{L-1}, T] \end{bmatrix}$$

Cost Model:

$$T(S^x) = FP(S^x) + BP(S^x)$$
$$M(S^x) = M_S(S^x) + M_D(S^x)$$

Bubble Overhead:

$$(B_R,\ B_I,\ B_P) = \mathcal{F}(FP(S^x),\ BP(S^x))$$

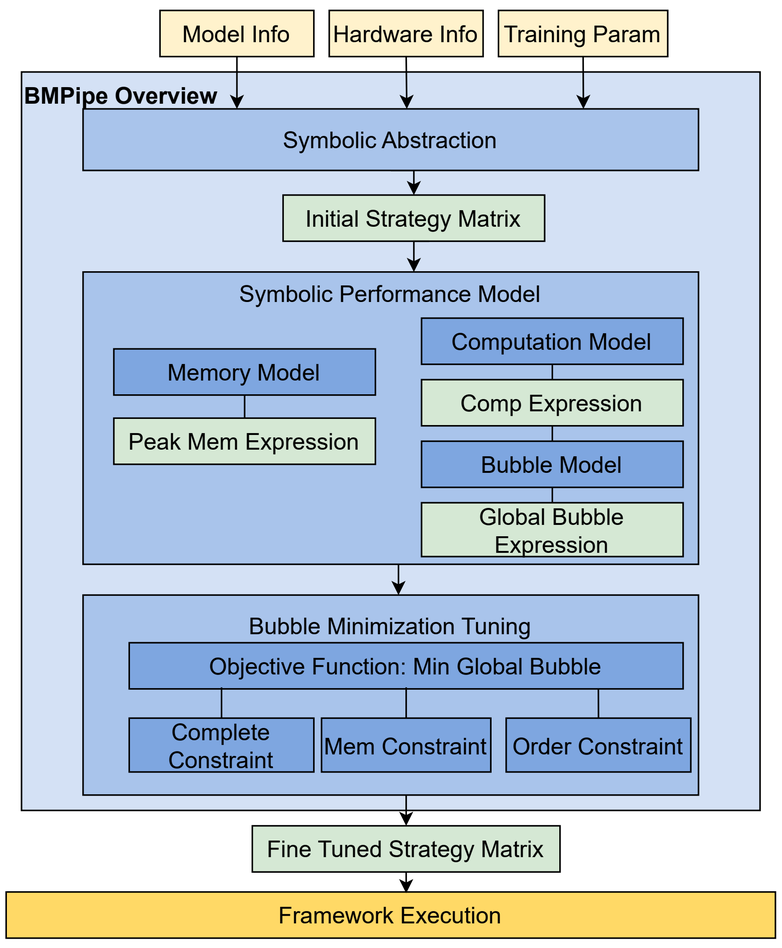
Constraints:

$$(C_i) = \mathcal{G}(FP(S^x),\ BP(S^x), M_S(S^x), M_D(S^x))$$

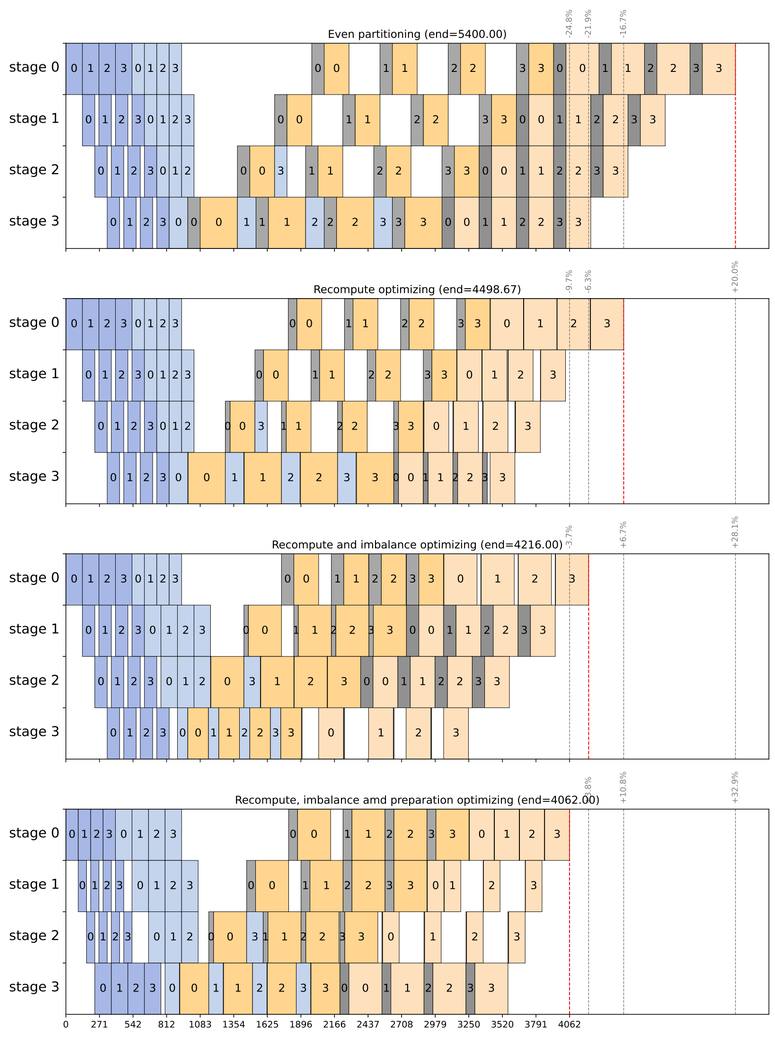
Algorithm 1: *Our planner*

Input: Layer set $\mathcal{L}$, recompute set $\mathcal{R}$; stages P; chunks C; device memory D_M; micro-batches μ
Output: Optimal assignment matrix S^*

```
// Phase 1: cost pre-computation
foreach distinct t ∈ T do
    (FP, BP) ←GetCompCost(t); M_S←GetMemCost(t);
foreach distinct (t, r) ∈ T × R do
    Recom ←GetCompCost(t,r); M_A←GetMemCost(t,r);
// Phase 2: ILP build
define l_{t,r,c,x} ∈ Z_{≥0}, b_{t−1,c,x} ∈ {0, 1};
minimize B_G = B_R + B_I + B_P;
add constraints C1, C2, C3;
// Phase 3: solve
solve ILP with Gurobi; obtain l*_{t,r,c,x}, b*_{t−1,c,x};
// Phase 4: build S*
foreach (t, r, c, x) do
    assign l*_{t,r,c,x} layers of type t to chunk c of stage x
      with strategy r;
return S*
```



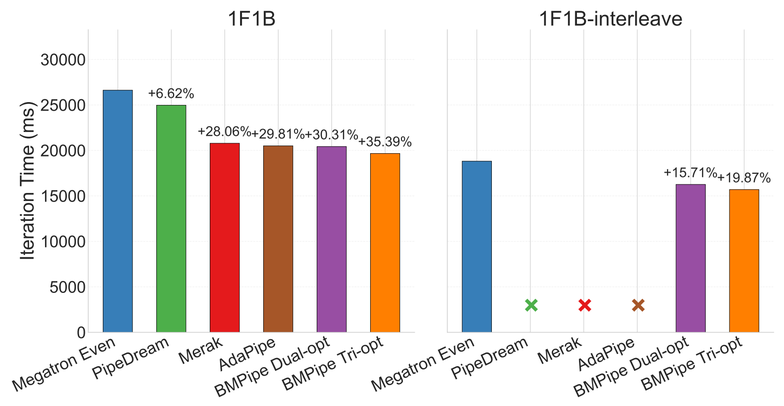
Running Example



Evaluation

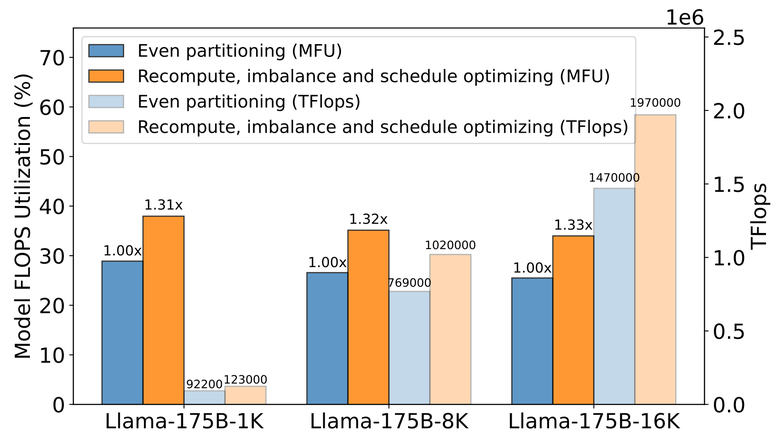
End-to-End performance

Experimental setup:
Bench-marked on a 16384× Ascend-910 NPU cluster (CANN 7.1, MindSpore 2.3) across 6 SOTA models: LLaMA-70/175B, BLOOM-176B, Qwen2-72B, Pangu-α-230B, LLaMA-MoE-1.04T, Multi-modal model-70B, against ***Megatron-Even***, ***PipeDream***, ***Merak***, ***AdaPipe***.

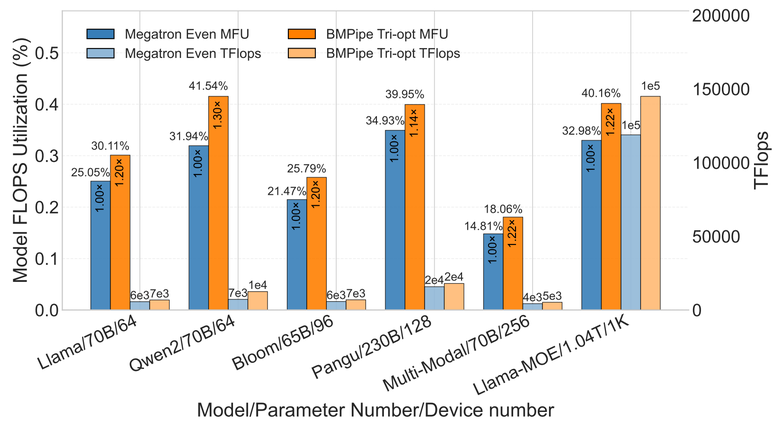


Very-large DNN model and cluster evaluation (LLaMA-175B @ 16k devices):

- *Vanilla 1F1B*: *PipeDream* 1.07 ×, *Merak* 1.29 ×, *AdaPipe* 1.30 ×, *Our Solution* dual/tri 1.31 × /1.36 × versus *Megatron-Even* (up to 36 % faster).
- *1F1B-Interleaved*: *Megatron-Even* is 1.41, × over vanilla; *Our Solution-Dual* adds 1.16 ×, tri 1.20 ×;
- 1.70 × *Our Solution* on 1F1B-Interleaved vs. Megatron-Even on vanilla.

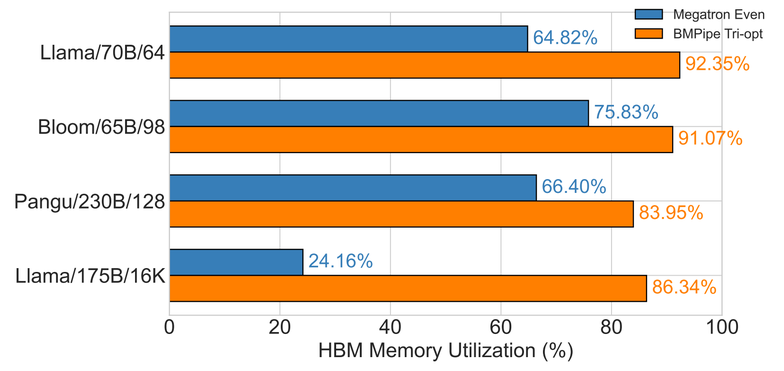


Scalability:
As device count scales **1,024 → 8,192 → 16,384**, *Our Solution-Tri* sustains 1.18 − 1.20 × speed-up; MFU climbs 28.4 % → 37.9 %.



Generality:
The MFU of six SOTA models increases by 1.20 − 1.31 ×.

Memory utilization



Memory Efficiency:
On 64–128-device runs, *Megatron-Even* taps only 64 − 75 % HBM; *Our Solution-Tri* raises this to 83 − 92 %, which equates to an effective capacity gain of 1.20 − 1.42 ×.

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